

Serial No.: 10/652,482
Docket No. NE304-US
TAK.045



AMENDMENTS TO THE SPECIFICATION

Please amend the specification as shown following:

In the paragraph beginning at line 20 on page 13:

Referring to FIG. 1, a disk array apparatus 1 according to an embodiment of the present invention connects to hosts A 91 and B 91 92 via host interfaces A 121 and B ~~121~~ 122. The disk array apparatus comprises a disk unit device 5, a ~~each~~ cache unit 6, a disk controller A 71, a disk controller B 72, a host controller A 81, and a host controller B 82.

In the paragraph beginning at line 2 on page 14:

The host controllers A 81 and B 82 perform host services such as command reception, data transfer, status response between the disk array apparatus and the hosts A 91 and B 92, respectively. The host controllers A 81 and B 82 connect to the ~~each~~ cache unit 6 and to disk controllers A 71 and B 72 through an inner bus 110, so as to perform data transmission/reception amongst each other. The host controllers A 81 and B 82 and the disk controllers A 71 and B 72 perform requests for processing such as disk processing to other controllers, and status information of controllers such as information of loop analysis result, via a ~~communicating~~ communication means between controllers 100[[],].

In the paragraph beginning at line 16 on page 17:

Referring to FIG. 1 again, the disk controller A 71 forms the FC-AL A 41 between only one port in each of the FC-AL disks 21 to 2N, and the other disk controller B 72 forms the FC-AL B 42 between the other port in each of the FC-AL disks 21 to 2N. The disk controllers A 71 and B 72 perform various disk processing such as reading from and writing to the FC-AL disks 21 to 2N with instructions from the host controllers A ~~71~~ 81 and B 82, or by their own determinations of the disk controllers A 71 and B 72. Further, the disk

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controllers A 71 and B 72 also instruct the enclosure service units A 51 and B 52 to bypass or release the bypass of the FC-AL disks 21 to 2N, and read information of bypass state and the like from the enclosure service units A 51 and B 52. Further, the disk controllers A 71 and B 72 include temporary degeneracy controllers A 710 and B 720, loop diagnostic units A 711 and B 721, and heartbeat transmitters A 712 and B 722, respectively.

In the paragraph beginning at line 16 on page 20:

Referring to FIG. 1, the host controllers A 81 and B 82 which received instructions from the hosts A 91 and B 92 recognize such necessary information as logic disk numbers (LUN), instruction code types, and logic block addresses (LBA). For example, the host controller A 81 and B 82 which received read instructions from the hosts A 91 and B 92, immediately transfer data from the ~~eash~~ cache unit 6 to the host A 91 and B 92, if the designated data exists in the ~~eash~~ cache unit 6. If the designated data does not exist in the ~~eash~~ cache unit 6, the host controllers A 91 and B 92 instruct the disk controllers A 71 and B 72 to store data read out from the FC-AL disks 21 to 2N in the ~~eash~~ cache unit 6, and when the data is stored in the ~~eash~~ cache unit 6, transfer the data to the host A 91 and B 92. Further, if the host controllers A 81 and B 82 received write instructions from the host A 91 and B 92, for example, they store the data received from the hosts A 91 and B 92 in the data in the ~~eash~~ cache unit 6. This data is written in the FC-AL disks 21 to 2N by the disk controllers A 71 and B 72, through instructions from the host controllers A 81 and B 82 to the disk controllers A 71 and B 72 to write the data into the disks, or through detection by the disk controllers A 71 and B 72 that unwritten data exists in the ~~eash~~ cache unit 6. Generally, the two disk controllers A 71 and B 72 are used to share the FC-AL disks 21 to 2N to which processing is assigned, so as to divide the loads.